# P P SAVANI UNIVERSITY

**Fourth Semester of B. Tech. Examination**

**May 2022**

**SECE2040 Computer Organization**

**25.05.2022, Wednesday** **Time: 09:00 a.m. To 11:30 a.m.** **Maximum Marks: 60**

***Instructions:***

1. The question paper comprises of two sections.
2. Section I and II must be attempted in same answer sheet.
3. Make suitable assumptions and draw neat figures wherever required.
4. Use of scientific calculator is allowed.

## SECTION – I

**Q - 1** Answer the Following: (Any Five) **[05]**

**(i)** What is the term used for "sequence of instructions for the computer"?

a. Hardware b. Program c. Data d. Instruction

**(ii)** What is concerned with the way the hardware components operate to form computer system?

a. Computer organization b. Computer design.

c. Computer architecture d. Computer implementation.

**(iii)** CMA is _____ type of instruction.

**(iv)** What is Assembler?

**(v)** What is 2's complement representation of -25 using 8-bits?

**(vi)** What is the use of PC (Program Counter) register in basic computer?

**(vii)** Perform Arithmetic Shift left on following binary number$(100110011)_2$

**Q - 2 (a)** Perform the following Conversion: **[05]**

a. $(93)_{10}$ to Binary b. $(9.AA)_{16}$ to Binary

c. $(623)_8$ to Hexadecimal d. $(101.011)_2$ to Decimal

e. $(3.F)_{16}$ to Decimal

**Q - 2 (b)** Explain Stored Program Organization with one processor register and an instruction code format with two parts. **[05]**

**OR**

**Q - 2 (a)** Perform the arithmetic operations in binary using signed-2's complement representation for negative numbers: (+42) + (-13) and (-42) – (-13) **[05]**

**Q - 2 (b)** Explain memory reference and register reference instruction code format with example. **[05]**

**Q - 3 (a)** Show the contents of register E, A, Q and SC during the process of multiplication of two binary numbers, 11111(multiplicand) and 10101(multiplier).The signs are not included. **[05]**

**Q - 3 (b)** Design a Flowchart for addition and subtraction of two binary numbers A and B. Assume that the numbers are stored in signed-magnitude representation. **[05]**

**OR**

**Q - 3 (a)** Show the contents of register E, A, Q and SC during the process of division of 10010011 by 1011.(Use a dividend of eight bits). **[05]**

**Q - 3 (b)** Multiply 5 with 3 using Booth algorithm. Show the step-by-step multiplication process. **[05]**

**Q - 4** List out the tables used during second pass of assembler. Draw flowchart to explain second pass of assembler. **[05]**

## SECTION – II

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|---|---|---|
| **Q - 1** | Answer the Following: (Any Five) | **[05]** |
| **(i)** | What is DMA? | |
| **(ii)** | IPC stands for _____. | |
| **(iii)** | How many 128*8 RAM chips are needed to provide a memory capacity of 2048 bytes? | |
| **(iv)** | Write down only name of six Phases in an Instruction Cycle. | |
| **(v)** | What is Virtual Memory? | |
| **(vi)** | Explain PIPELINING in short. | |
| **(vii)** | Difference between Volatile & Non-Volatile memory. | |
| **Q - 2 (a)** | What do you mean by Priority Interrupt? Explain the stage of daisy-chain priority Arrangement in details. | **[05]** |
| **Q - 2 (b)** | Explain the connection of I/O bus to input-output device? What are the various types of commands that are received by I/O interface for particular I/O device? | **[05]** |
| | **OR** | |
| **Q - 2 (a)** | Explain about Cache Coherence in detail. | **[05]** |
| **Q - 2 (b)** | What is the purpose of Input-Output Interface? What are the differences between CPU and I/O Device that can be resolved by Input-Output Interface? | **[05]** |
| **Q - 3 (a)** | Differentiate the following:<br>Synchronous Data Transfer vs. Asynchronous Data Transfer | **[05]** |
| **Q - 3 (b)** | Draw a neat diagram of memory hierarchy of computer system. Also indicate relative variation of size, speed and cost per bit in the hierarchy. | **[05]** |
| | **OR** | |
| **Q - 3 (a)** | Differentiate the following:<br>Source-initiated Strobe vs. Destination-initiated Strobe | **[05]** |
| **Q - 3 (b)** | What is main Memory? Draw the block diagram and function table of typical RAM chip (128*8) and ROM chip (512*8). | **[05]** |
| **Q - 4** | Attempt any one. | **[05]** |
| **(i)** | What is parallel processing? How Parallel Computers are classified based on Flynn's classification? | |
| **(ii)** | What do you mean by Peripherals? Explain about various types of peripherals? | |

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